Amendments to the Specification

Please amend paragraph [0028] as follows:

[0028] A novel hardware mechanism labeled herein Packet Predictor 202 is provided within system [[202]] 201 and enables prediction of data packet characteristics before some packets actually arrive through ingress of the processing system. Data packet predictor 202 is a front-end hardware implementation that generates speculative packet information for a virtual data packet (predicted data packet). A packet prediction may be triggered by any one of several events and conditions, such as detection of idle processor time. A good time, however, and a trigger used in a preferred embodiment is when a real data packet is received by the processing system.

Please amend paragraph [0029] as follows:

[0029] Packet predictor 202 has, in this example, a dedicated memory (MEM) 204 provided therein and adapted to store historical data regarding real data packets previously processed within the system and historical data about successful instances of predicted data packets within the system, wherein the speculative processing results associated with a predicted packet, backed up by a real packet, were correct enough to send the real packet out of the system requiring little or no processing of the information associated with the real packet. MEM [[202]] 204 can be a flash type MEM, ROM, RAM, or any other type of usable memory sufficient in size to hold at least a historical record covering a pre-defined number of data packets.

Please amend paragraph [0030] as follows:

[0030] In a preferred embodiment, MEM [[202]] 204 stores a revolving history record that is updated periodically, whether or not the processing was "real" or "virtual". For example, MEM [[202]] 204 may store historical data covering the last 10 data packets received, and also the practical result of the last ten data packets predicted. In other embodiments the history record could cover many more, or fewer data packets, both real and virtual. In an alternative embodiment of the invention, MEM [[202]] 204 may be implemented externally from predictor 202 or from buffer system 201, or even externally from the router without departing from the spirit and scope of the present invention. For example, MEM 204 may be an assigned portion of existing memory within the processing system such as queue memory or processing core memory. There are many possibilities.